REMARKS

The Examiner is thanked for withdrawing the previous rejections of in response to Applicant's Amendment filed April 7, 2009.

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Rejections under 35 U.S.C. §112

With respect to the rejection of claim 1 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, Applicant has amended claim 1 to correct a typographical error by deleting "when" in the phrase "when from an input side." Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection.

2. Rejections of claim 1-2, 4-5, 7-8, and 10-15 under 35 U.S.C. §103(a)

With respect to the rejection of claims 1-2, 4-5, and 7-8 are rejected under 35 U.S.C. §103(a) as being unpatentable over LeBlanc (US 2004/0057445) in view of Kramer (US 6,658,027), to the rejection of claims 10 and 12-15 under 35 U.S.C. §103(a) as being patentable over LeBlanc, Kramer and in further view of Gladden (US 6,738,916), and to the rejection of claim 11 under 35 U.S.C. §103(a) as being patentable over LeBlanc, Kramer, Gladden, and in further view of Otlean (US 6,044,113), Applicant respectfully traverses the rejections at least for the reason that LeBlanc, Kramer, Gladden, and Otlean, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claims.

In a controlling method and a control device according to the present inventions, a jitter buffer (FIFO) is set with a packet delete area, a packet add area, and a clock control area. The packet add area has an upper limit (T1). The packet delete area has a lower limit (T4). The clock control area has a lower limit (T2) and an upper limit (T3). The upper limit (T1) of the packet add area is lower than the lower limit (T2) of the clock control area. The lower limit (T4) of the packet delete area is high than the upper limit (T3) of the clock control area. Accordingly, even if packet data quantity in the jitter buffer exceeds the upper limit (T3) of the clock control area, the packet data is not deleted at once. And, even if packet data

quantity in the jitter buffer falls below the lower limit (T2) of the clock control area, the packet data is not added at once.

Accordingly, the present invention has advantages as described in the specification, particularly in page 6, lines 22 to page 7, line 18.

In contrast with Applicant's claimed invention, LeBlanc describes a jitter buffer that utilizes different criteria to process voice packets in the jitter buffer. More specifically, instead of controlling the jitter buffer based on the physical limits (e.g., upper limit T1, lower limit T4 of packet add/delete areas and upper limit T2 and lower limit T3 of clock control area) as in the presently claimed invention, LeBlanc controls the jitter buffer based on how long (i.e., holding time) a packet has been stored in the buffer.

In paragraph [0033] of LeBlanc, which is cited by the Examiner as describing a clock control area inside the jitter buffer ("FIFO"), LeBlanc merely describes holding time thresholds and changing the retrieval rate based on whether the holding time thresholds are met. Although LeBlanc discusses, e.g., "the higher the holding time, the higher the retrieval rate", there is no relationship between LeBlanc's holding time thresholds and retrieval rate and Applicant's clock control area's lower limit (T2) and upper limit (T3) and raising/lowering a clock frequency based on the packet's level in the clock control area.

In other words, LeBlanc's holding time threshold is related to how long a packet has been in the jitter buffer and is unrelated to Applicant's claimed physical level (e.g., T2, T3) of the clock control area in the FIFO buffer. Further, LeBlanc does not teach, disclose, or suggest changing the clock frequency to change the retrieval rate.

Further, as acknowledged by the Examiner, LeBlanc does not teach, disclose, or suggest deleting/storing packet based on the limits in packet delete/add areas. Applicant respectfully points out to the Examiner that because LeBlanc's reliance on the holding time of packets and moving the packet from the jitter buffer at an adjusted rate based on a holding time threshold, LeBlanc inherently does not delete packet from the jitter buffer. That is, if a packet were deleted from the jitter buffer of LeBlanc, then there would no need to rely on or to determine a holding time of a packet in the jitter buffer. Applicant respectfully submits that LeBlanc does not teach, disclose, or suggest deleting a packet from the jitter buffer.

With respect to Kramer, the Examiner cited Kramer as curing the acknowledged deficiencies of LeBlanc. The Examiner contends that controlling the stored quantity to delete specified packets as recited in Applicant's claims is well-known, using Kramer as a

secondary reference. However, LeBlanc does not teach, disclose, or suggest controlling packets in a buffer by deleting specified packets. As asserted above, LeBlanc's reliance on holding time necessitates a packet to be present and its holding time kept. Deleting a packet (or discarding a frame) as taught in Kramer would be contrary to LeBlanc's reason for relying on the holding time of a packet and changing the retrieval rate based on the time a packet has been in the jitter buffer.

In view of the above, Applicant respectfully submits that LeBlanc and Kramer, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claim independent claim 1 and its dependent claim 2, 4-5, and 7-8.

The arguments set forth above in relation to claim 1 directed to a method, are also applicable to the rejection of device claim 10 and its dependent claims 11-15 and Applicant's additional arguments set forth below with respect to Gladden and Otlean.

Gladden is directed to a method for emulating a clock signal. The Examiner relies on Gladden as teaching a VCO that provides a clock frequency that can be varied. However, similar to Kramer, Gladden also fails to cure the above-mentioned deficiencies of LeBlanc, as Gladden fails to teach, disclose, or suggest, for example, a buffer control circuit to control the quantity of packets accumulated in the FIFO to delete the packets when the stored packet quantity exceeds a lower limit of a packet delete area, as recited in claim 10.

Otlean, on the other hand, generally describes a digital pulse with modulator, which is completely different subject matter than the presently claimed invention and has no resemblance structurally or functionally to Applicant's device recited in claim 10 and its dependent claim 11. Further, similar to Gladden and Kramer, Otlean also fails to cure the above-discussed deficiencies of LeBlanc, as Otlean fails to teach, disclose, or suggest, for example, a buffer control circuit to control the quantity of packets accumulated in the FIFO to delete the packets when the stored packet quantity exceeds a lower limit of a packet delete area, as recited in claim 10.

In view of the above, Applicant respectfully submits that LeBlanc, Kramer, Gladden, and Otlean, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claim independent claim 1 and its dependent claim 10-15.

3. Conclusion

In view of the amendments to the claims, and in further view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it

is requested that claims 1-2, 4-5, 7-8, and 10-15 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Further, while no fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

/Donald R. Studebaker/
Donald R. Studebaker
Registration No. 32,815

Studebaker & Brackett PC
One Fountain Square
11911 Freedom Drive
Suite 750
Reston, Virginia 20190
(703) 390-9051
Fax: (703) 390-1277
don.studebaker@sbpatentlaw.com